REMARKS

By this amendment, Applicants have amended claims 1, 8, 10-11, 13-15, 21, and 28. As a result, claims 1-3, 7-8, 10-11, 13-17, 20-21, 23-26, and 28-29 remain pending in this application. These amendments are being made to clarify the presently claimed subject matter, and are not being made to overcome the rejections included in the Office Action. Applicant does not acquiesce in the correctness of the objections and rejections and reserves the right to pursue the full scope of the subject matter of the original claims, or claims that are potentially broader in scope, in the current and/or a related patent application. Reconsideration in view of the following remarks is respectfully requested.

In the Office Action, the Office objects to the drawings for allegedly failing to show every feature of the invention specified in the claims. In particular, the Office alleges that the drawings fail to show a field effect transistor array and an array of rectifying contacts as in claim 1. However, Applicants note that FIG. 2 shows an illustrative field effect transistor, and FIGS. 7 and 8 show illustrative arrays of heterodimensional diodes. The application further discusses arrays of various devices, including field effect transistors. Specification, paragraph 0035. To this extent, Applicants respectfully submit that a person having ordinary skill in the art would understand the claim term "field effect transistor array" without the aid of an additional figure. Similarly, FIG. 8 shows multiple rectifying contacts included in an array of heterodimensional diodes. To this extent, Applicants respectfully submit that a person having ordinary skill in the art would understand the claim term "array of rectifying contacts" without the aid of an additional figure. As a result, Applicants respectfully request withdrawal of the objection to the drawings.

Further, the Office rejects claim 11 under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 6,269,199 (Maloney). Applicants respectfully submit that the Office fails to present a *prima facie* case of anticipation. For example, the Office fails to show that Maloney discloses shining a laser pulse onto a field effect transistor as in claim 11. In support of its rejection, the Office cites col. 7, lines 5-6 of Maloney as allegedly disclosing this feature. However, Applicants note that this portion of Maloney discloses use of "a coherent laser beam". As shown in FIGS. 1, 2, and 4 of Maloney, the laser beam is continuous, not pulsed. In sharp contrast, Applicants shine a laser pulse in claim 11, which inherently has a short duration.

Additionally, the Office fails to show that Maloney discloses adjusting a frequency of radiation to a desired frequency by adjusting a carrier density of carriers in a channel of a field effect transistor as in claim 11. In support of its rejection, the Office cites several portions of Maloney. However, Applicants note that none of the cited portions discuss adjusting a frequency of radiation at all. To the contrary, Maloney merely discloses a causing an optical phase shift of reflected light. See, e.g., Maloney, Abstract, FIGS. 1, 2, and 4; col. 4, lines 32-37. Applicants note that shifting the phase of light is clearly distinct from and does not anticipate adjusting a frequency of radiation as in claim 11.

In light of the above, Applicants respectfully request withdrawal of the rejection of claim 11 as allegedly being anticipated by Maloney. However, should the Office maintain its rejection, Applicants respectfully request that the Office further discuss and clarify how Maloney allegedly discloses adjusting a frequency of radiation to a desired frequency as in claim 11.

Further, the Office rejects claims 1-3, 7-8, 10, 13-17, 20-21, 23-26, and 28-29 under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,371,388 (Oda) in view of U.S. Patent No. 5,729,017 (Brener).

With respect to claim 1, Applicants respectfully submit that the Office fails to establish a *prima facie* case of obviousness. For example, the Office fails, *inter alia*, to show that Oda teaches adjusting a frequency of the radiation to a desired frequency using a voltage applied to the semiconducting device as in claim 1. In support of its rejection, the Office cites the Abstract of Oda as allegedly teaching this feature. Office Action, p. 5. However, Applicants note that Oda's Abstract does not include any discussion of adjusting a frequency of radiation to a desired frequency, let alone doing so using a voltage applied to a semiconducting device as in claim 1. In sharp contrast, Oda teaches modulation of the gate voltage to attain modulation of a current amplitude, see, e.g., Oda, col. 7, lines 43-46, and setting a voltage according to an intensity of light to be detected, see, e.g., Oda, col. 10, lines 15-28. Applicants note that the intensity of light and the current amplitude are unrelated to the frequency of the radiation. As a result, Applicants respectfully submit that Oda fails to teach or suggest adjusting a frequency of the radiation to a desired frequency using a voltage applied to the semiconducting device as in claim 1.

In response to Applicants previous arguments, the Office asks "just what the heck... a 'heterodimensional diode' is." Office Action, p. 7. The Office defines the term as "a contact of dissimilar dimensions forming a p-n junction in a semiconductor wafer", and alleges that Oda's FIG. 12 features two such contacts. Office Action, p. 8. Even if, *arguendo*, the Office's definition of 'heterodimensional diode' is accurate, the Office's interpretation of the definition and application of the definition to the teachings of Oda are in error. Oda's device in FIG. 12 is shown including conventional top-grated ohmic contacts 21, 23, each of which includes a corresponding diffused region 36, 37, respectively. The diffused regions 36, 37 are formed by a thermal treatment of the device, which is typically done with ohmic contacts to lower a barrier at the contact interface. Oda shows diffused regions 36, 37 contacting electron gas 30 in the device.

However, the diffused regions 36, 37 are not "contacts of dissimilar dimensions" as the term is used in the art, and particularly as it is used in the article by Nabet et al., titled "Heterojunction and heterodimensional devices for optoelectonics", which was published in Microwave Magazine in March 2001 ("Nabet"), and is used by the Office to form its definition. In particular, a heterodimensional contact is formed when a one- or two-dimensional system is contacted by a higher dimensional system (e.g., three-dimensional), which forms a barrier for the electrons/holes in the lower dimensional system. In fact, Nabet supports Applicants' position that the device in Oda does not include any heterodimensional contacts and that "heterodimensional" devices are known in the art. In particular, Nabet compares operation of devices with ohmic and Schottky surface contacts to the 2DEG with operation of a device with Schottky heterodimensional contacts. In FIG. 2, a device with ohmic contacts to the 2DEG is shown, and in FIG. 4, a device with Schottky contacts is shown. As illustrated, the ohmic and Schottky contacts are on a surface of a spacer layer in the respective devices, similar to contacts 21, 23 of Oda's device. Additionally, the ohmic contacts in FIG. 2 include diffused regions underneath, similar to the contacts in Oda's device. In FIG. 7 of Nabet, a device with Schottky heterodimensional contacts is shown. As illustrated, the Schottky heterodimensional contacts form a lateral junction with the 2DEG. Nabet, FIG. 7. Nabet contrasts operation of the heterodimensional device with operation of the devices that include surface contacts and concludes that the operation of the devices are qualitatively different. Nabet, pp. 41, 44-45. For example, the heterodimensional device was shown to improve dark current as well as light response and have an increased barrier height. Nabet, p. 41, col. 1, lines 41-46; p. 45, col. 2, lines 8-9.

Additionally, in an Exhibit for this response, Applicants have provided the Office with another illustrative paper on heterodimensional devices and their differences from prior art devices. In the paper by Hurt et al., titled "Heterodimensional Device Technologies", which was published in Compound Semiconductor in March/April 1997 ("Hurt"), conventional Schottky contacts and heterodimensional Schottky contacts are compared. See, e.g., Hurt, p. 35, Figure 2. Applicants note that both Hurt and Nabet use the same definition for heterodimensional contacts/devices, and both Hurt and Nabet show contacts similar to those of Oda and describe these contacts as being distinct from heterodimensional contacts.

Further, Applicants note that the Specification of the current application uses the same definition of heterodimensional contacts/devices as used in Hurt and Nabet. For example, FIG. 6 is shown and described as showing a heterodimensional diode, which includes "[a]n active layer 416 that includes a two-dimensional carrier gas (electron or hole), and is bounded by a contact on one side and a second contact on another side." Specification, paragraph 0032. Contact 436 is described as a rectifying contact that forms a p-n junction with the two-dimensional carrier gas, resulting in the formation of a horizontal depletion region. See, e.g., FIG. 6; paragraph 0032. Still further, Applicants note that U.S. Patent Application Publication No. 2004/0188703 ("Cheng"), which is briefly alluded to by the Office, also uses the same definition of heterodimensional contacts/devices as used in Hurt, Nabet, and Applicants' Specification. For example, FIG. 1 of Cheng is described as showing a switch 1 that comprises a heterodimensional FET structure, which includes a source 2 and drains 3(a), 3(b), which form junctions with a 2D hole channel 5, and cause the formation of horizontal depletion regions during operation. See, e.g., paragraphs 0027-0033, 0040.

In light of the above articles and patent applications, Applicants respectfully submit that the terms "heterodimensional contacts" and "heterodimensional devices" have long used (dating back at least as early as 1997, more than six years prior to Applicants' filing of the present application), well understood meanings by those in the semiconductor industry. Additionally, the Office alleges "that the mainstream semiconductor industry (including Oda and Brener et al.) has stubbornly resisted efforts to popularize the term 'heterodimensional'". Office Action, p. 9. However, Applicants note that the lack of use of the term "heterodimensional" in Oda and Brener is, at least in part, due to the lack of discussion of any heterodimensional contact/device in either reference. Regardless, should the Office require additional references in support of Applicants' contention that heterodimensional contacts/devices are understood by those in the mainstream semiconductor industry, Applicants can provide the Office with further background publications.

In further response to Applicants' previous arguments, the Office alleges that

> Applicants are confusing a step (applying a voltage to the semiconducting device) that may be performed by a device under the control of an individual, with the result (radiation has its frequency adjusted) achieved by the performance of said step. In a device (such as Oda's) of the sort used to perform the claimed method, characteristics of the two-dimensional carrier gas, once modified by adjusting the applied voltage, inevitably adjust the frequency of the radiation generated by the device.

Office Action, p. 10. (emphasis in original)

Initially, Applicants note that the device in Oda is not disclosed as being "of the sort used to perform the claimed method" as alleged by the Office. In particular, as noted above, Oda fails to teach or suggest adjusting a frequency of radiation at all, which is included in the method of claim 1, let alone doing so in the manner described in claim 1. Further, as also discussed above, Oda fails to disclose a heterodimensional diode as alleged by the Office. Still further, Applicants have amended claim 1 to expressly state that the frequency is adjusted to a desired frequency,

which cannot be inherently performed by any device. As a result, Applicants submit that the Office fails to present a sufficient showing that Oda describes any type of "device... of the sort used to perform the claimed method..." as alleged in the Office Action. However, should the Office maintain this holding, Applicants request that the Office further describe how the device in Oda is a heterodimensional diode and is described as being used in a process that adjusts a frequency of the radiation to a desired frequency using a voltage applied to the semiconducting device as in claim 1.

The Office goes on to state that "[u]nder the principles of inherency, if a prior art device, in its normal and usual operation, would necessarily perform the claimed method, then the method claimed will be considered to be anticipated by the prior art device." Office Action, p. 11. However, as discussed above, Oda does not show any of the devices of claim 1. Further, Applicants have expressly claimed that the frequency is adjusted to a desired frequency, which is not inherent in the operation of any device. As a result, Applicants submit that the Office fails to present a *prima facie* showing of inherency. Applicants note that the combination of Oda with Brener, even if, *arguendo*, proper, fails to address the deficiencies discussed herein with respect to Oda.

In light of the above, either alone or in combination, Applicants respectfully request withdrawal of the rejections of claim 1 and claims 2-3, 7, and 23-24, which depend therefrom, as allegedly being unpatentable over Oda in view of Brener.

With respect to independent claims 8, 10, 13-15, 21, and 28, Applicants note that the Office relies on its inherency argument presented above with respect to claim 1 in each of these rejections. To this extent, Applicants have amended each of these claims to expressly state "adjusting a frequency of the radiation to a desired frequency". Applicants note that such an

action cannot be inherently shown in any reference. As a result, Applicants respectfully request withdrawal of the rejections of claims 8, 10, 13-15, 21, and 28, and any dependent claims thereof, as allegedly being unpatentable over Oda in view of Brener.

With further respect to claim 8, the Office alleges that "'adjusting a gate length,' in the context of Applicants' claims, means nothing more or less than the process of setting aside a device having a particular gate length and picking up a different device that happens to have a different gate length." Office Action, p. 14. However, Applicants respectfully submit that the Office improperly reads limitations from the specification into the claims to form this conclusion. Applicants respectfully submit that the claims are not limited to merely using devices of different gate lengths. To the contrary, the claims should be interpreted to include any solution for adjusting a gate length, including an effective gate length, for the gate that is known in the art.

With further respect to claims 21 and 28, Applicants note that the Office alleges that neither claim recites "a field effect transistor having a periodic grating gate". Office Action, p. 19. However, Applicants note that on lines 2-3 of each claim, "providing ***a field effect transistor having*** a two-dimensional carrier gas and ***a periodic grating gate***" is claimed. As a result, Applicants again respectfully request withdrawal of the rejections of claim 21 and 28 in light of the previously presented arguments.

Finally, Applicants' undersigned attorney respectfully requests that the Examiner, in future correspondence, conduct business using the same decorum and courtesy that Applicants and Applicants' undersigned attorney are required to use and have used in conducting business with the Office. See, e.g., 37 CFR 1.3. In particular, Applicants' attorney respectfully requests that the Examiner refrain from further: (a) use of slang in the correspondence; (b) assigning motives to Applicants' use of terminology; (c) identifying and characterizing alleged

actions/inactions by the mainstream semiconductor industry; and (d) negatively characterizing Applicants and their colleagues, all of which are included in the current Office Action. Applicants are well published, highly distinguished researchers and businessmen in the semiconductor industry and should not be subjected to such disrespectful conduct while seeking to protect their unique inventions.

Applicants submit that each of the pending claims is patentable for one or more additional unique features. To this extent, Applicants do not acquiesce to the Office's interpretation of the claimed subject matter or the references used in rejecting the claimed subject matter. Additionally, Applicants do not acquiesce to the Office's combinations and modifications of the various references or the motives cited for such combinations and modifications. These features and the appropriateness of the Office's combinations and modifications have not been separately addressed herein for brevity. However, Applicants reserve the right to present such arguments in a later response should one be necessary and/or in a related patent application, either of which may seek to obtain protection for claims of a potentially broader scope.

In light of the above, Applicants respectfully submit that all claims are in condition for allowance. Should the Examiner require anything further to place the application in better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the number listed below.

Respectfully submitted,

/John LaBatt/

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EXHIBIT

Heterodimensional Device Technologies

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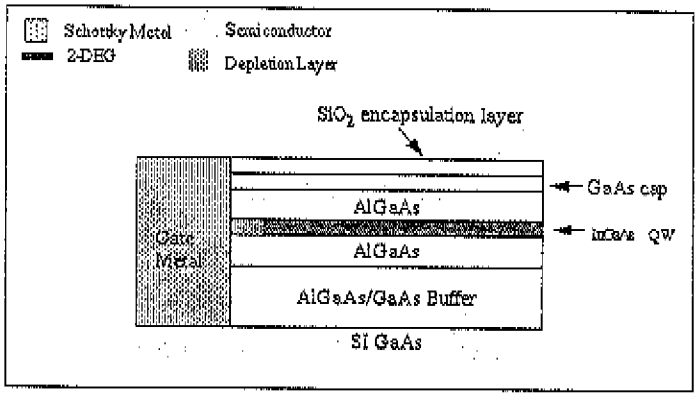

Figure 1. A heterodimensional interface is an interface between two regions of different dimensions, such as the contact between a Schottky gate and a thin InGaAs quantum well (QW) layer shown above.

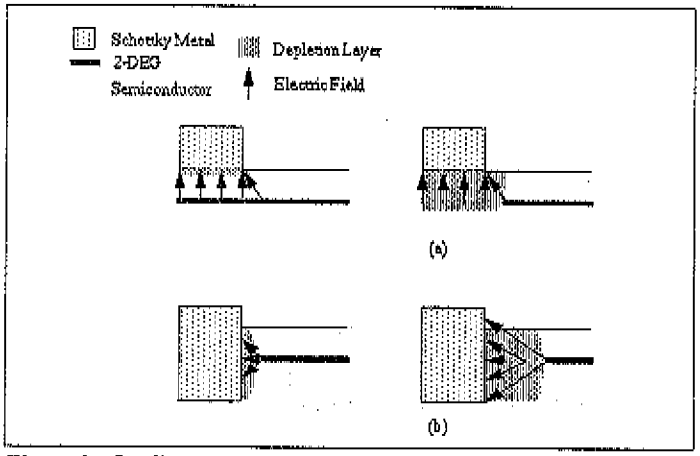

Figure 2. Qualitative comparison between (a) conventional top-gated contacts and (b) heterodimensional contacts. Illustration shows contacts under zero bias (left) and negative bias (right). The unit-width capacitance of the heterodimensional 3d/2d junction is low due to the small effective cross section of the metal/2-DEG interface.

Heterodimensional semiconductor devices are steadily emerging as an exciting new class of devices with a wide variety of applications including two-terminal device frequency multiplication, three-terminal device optoelectronic detectors, and four-terminal device low power multi-functional digital logic integrated circuits. The term *heterodimensional* refers to a contact between semiconductor regions of different dimensions, such as a sidewall metal gate contacting the edge of a very thin conducting layer in an epitaxially grown heterostructure (see Figure 1). Heterodimensional contacts have unique electronic and geometric properties which provide a larger depletion width, smaller capacitance, higher breakdown voltage, and superior electron confinement compared to conventional semiconductor device structures. In addition, the novel side gate geometry allows for deep submicron scaling of both the gate length and channel width of heterodimensional field effect transistors. Together, the electronic and geometric properties of these devices offer exciting potential for innovative applications in millimeter wave, optoelectronic, and low power electronic circuits. In the following, we discuss the fabrication, performance, and emerging applications of heterodimensional device technology. We begin the discussion with an overview of heterodimensional interfaces.

Heterodimensional Interfaces

All semiconductor devices utilize interfaces between different regions or materials. Examples of common interfaces include p-n junctions, ohmic contacts, Schottky barriers, and heterojunctions. Typically, these interfaces are between two planar regions of comparable dimensions. Heterodimensional devices, however, utilize the interface between two semiconductor regions of different dimensions. An example of such an interface is the 3d/2d Schottky contact between a large (three-dimensional) metal area and a thin conducting layer of quantized electrons known as a two-dimensional electron gas (2-DEG). Other configurations are possible, such as the interface between a three-dimensional metal and a quantum wire (3d/1d junction) or even between a quantum wire and a two-dimensional metal strip (2d/1d junction). The heterodimensional semiconductor devices reported so far in literature employ, for the most part, the 3d/2d interface between a sidewall Schottky metal and the 2-DEG layer in an AlGaAs/ GaAs or AlGaAs/InGaAs heterostructure material structure (see Figure 1).

The heterodimensional 3d/2d contact provides a larger depletion width, smaller capacitance, higher breakdown voltage, and superior electron confinement than conventional semiconductor device structures. In conventional top-gated structures, such as HFETs, MOSFETs, or surface point-contact (split-gate) devices, modulation of the electron channel is controlled by an electric field perpendicular to the conducting layer, as illustrated in Figure 2(a). The capacitance in these structures scales with the parallel-plate area of the metal/semiconductor interface and is limited by the fringe capacitance. On the other hand, the unit-width capacitance of the heterodimensional 3d/2d junction is much lower due to the smaller effective cross section of the metal/2-DEG interface. The interface electric field of the heterodimensional contact is perpendicular to the *edge* of the 2-DEG, as shown in Figure 2(b), and the channel is modulated directly by the sidewall gate. The two-dimensional spreading of the lateral electric field distribution provides a wider depletion region and, consequently, a higher breakdown voltage than conventional structures. The "electrically pliable" 3d/2d junction has increased electrostatic damage immunity, an important feature for integrated circuit applications. In addition, the strong lateral field between the metal and the 2-DEG confines electrons better than surface contact devices, a feature which is important for quantum wire or quantum dot operation.

Heterodimensional Devices

Several different heterodimensional devices, including the Schottky metal/2-DEG diode, the 3d/2d metal/semiconductor field effect transistor (2d MESFET), the multi-channel microwave 2d MESFET, and the Schottky-gated resonant tunneling transistor (SG RTT), have been fabricated. In this article we provide a brief description of the Schottky metal/2-DEG diode and the 2d MESFET, and discuss potential applications.

Schottky metal/2-DEG diode

Prototype devices for the first heterodimensional device3-4 the Schottky/2-DEG diode, developed in 1991 at the University of Virginia3-4 were fabricated using an etch-and-plate method on a pseudomorphic $Al_{0.25}Ga_{0.75}As/In_{0.15}Ga_{0.85}As$ heterostructure. The heterostructure, grown by MBE, had an electron sheet charge density of 1.85×10^{12} cm^{-2} and electron mobilities of 6640 and 31400 cm^2/Vs at 295 and 77 K, respectively. Ohmic contacts on the diodes consisted of an electroplated SnNi/Ni/Au trilayer alloy. The heterodimensional gate contact was formed by first etching through the 2-DEG down to the buffer layer and then electroplating Pt/Au into the resulting trench.

The capacitance-voltage characteristics of a 100 μm wide Schottky metal/2-DEG diode varactor included a capacitance per unit width of less than 0.5 fF/μm, suggesting great potential for high speed operation. The diode was evaluated in a waveguide circuit as a frequency tripler to 225 GHz and a maximum efficiency of 1.24% was obtained at 35 mW input. While this efficiency is lower than that achieved in state-of-the-art GaAs multiplier diodes, these results indicate that the Schottky/2-DEG diode is capable of operation in millimeter and possibly submillimeter wavelengths following further optimization of the device. The two-terminal Schottky metal/2-DEG contact is a fundamentally new contact technology and it is the essential feature of the new heterodimensional three and four terminal devices, which are discussed next.

2d MESFET

Heterodimensional 3d metal/2-DEG field effect transistors (2d MESFETs), reported in 1993 by the University of Virginia group and in 1994 by a group from Hokkaido University in Japan, have been fabricated in a manner similar to the Schottky metal/2-DEG diode. The 2d MESFET utilizes the Schottky metal/2-DEG junction to laterally modulate the current flowing between drain and source. A bird's eye view illustration of the device is shown in Figure 3. Prototype devices, reported at the IEEE/Cornell Conference in 1993 by the University of Virginia group, were fabricated on a pseudomorphic $Al_{0.25}Ga_{0.75}As/In_{0.2}Ga_{0.8}As$ material structure. Room temperature transconductance values of 295 and 120 mS/mm were later achieved for 1.0 and 0.5 μm wide devices, respectively. The current-voltage characteristics of a typical 0.5 μm wide device are shown in Figure 4. Key features of this device include a low knee voltage (0.25 V), low peak current (45 μA at V_{GS}=0.6 V), low output conductance (less than 1 mS/mm), small DIBL voltage shift (less than 50 mV/V), large ON/OFF ratio (up to 10^7), and low leakage current (less than 1 nA at V_{DS}=50 mV). The narrow channel effect (NCE), which leads to parasitic currents at the gate edges in a top-gated structure, is eliminated in the 2d MESFET by the unique sidewall gate geometry, as evident by the low output conductance and small DIBL shift. In fact, the 2d MESFET has the unique feature that most of the electrical characteristics actually improve upon scaling to deep submicron dimensions.

Quantum Well Wire Applications

The geometry of the 2d MESFET lends itself ideally to quantum well wire (QWW) transistor applications. Researchers from Hokkaido University have demonstrated QWWs using $Al_{0.3}Ga_{0.7}As/GaAs$ 2d MESFETs, also called In-Plane Gate Transistors. Their work showed quantization (in units of $2e^2/h$) at 4 K with the first plateau visible up to 40 K for devices with channel lengths of 1.6 μm and widths between 0.4 and 0.7 μm. They also performed Shubnikov-de Haas measurements and, by plotting the Landau index level N vs. inverse magnetic field, found that the sheet carrier density is almost independent of gate bias, indicating that the side gates modulate the effective width of the channel but not the sheet carrier density. This result demonstrates that the geometry of the 2d MESFET provides better electron confinement than split gate structures, which are traditionally used for quantum wire or quantum point contact operation.

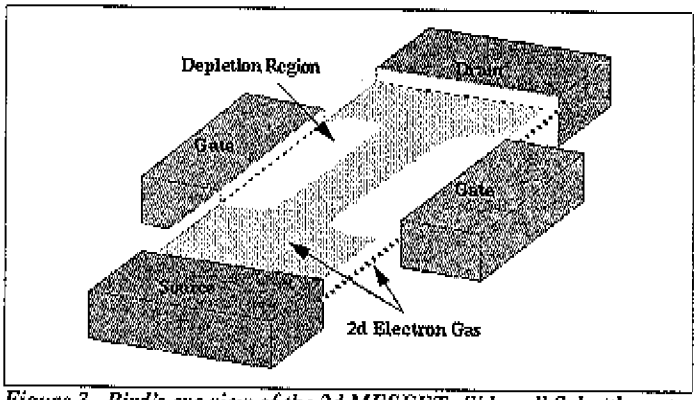

Figure 3. Bird's eye view of the 2d MESFET. Sidewall Schottky gates (red) modulate the 2-DEG electron channel (green) and laterally control the current flowing between source and drain.

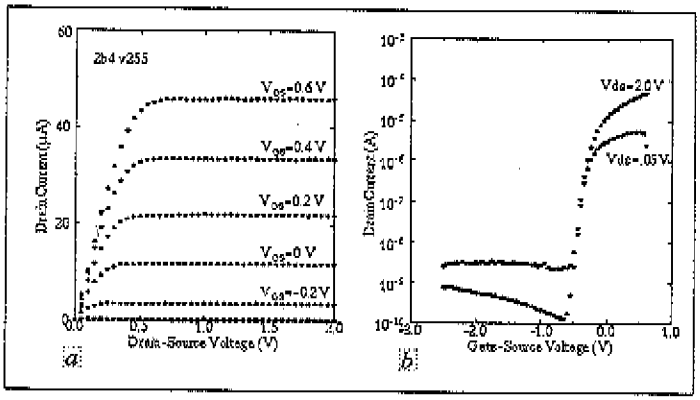

Figure 4. Typical DC current-voltage characteristics of a 2d MESFET having gate length and gate-to-gate width of 0.5 μm. (a) Drain current vs. drain-source voltage, and (b) drain current vs. gate-source voltage showing subthreshold behavior.

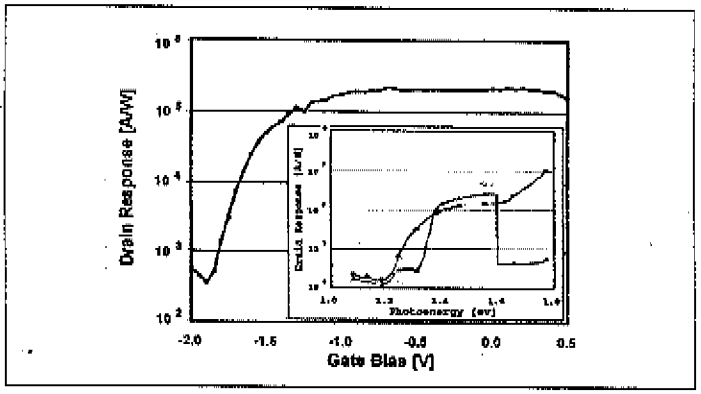

Figure 5. The 2d MESFET provides photoresponse under both top and backside illumination. The drain response of the 2d MESFET as a function of gate bias under backside-illumination of monochromatic light (900 nm) is shown above. In the inset, the drain photoresponse under top-illumination for gate bias of -1.0 V (circles) and -2.5 V (triangles) is shown for a drain bias of 1.0 V.

Photoelectric Response

The optoelectronic properties of the 2d MESFET have also been investigated. Researchers at the University of Virginia have examined the photoelectric response of the 2d MESFET under both top and bottom illumination. The geometry of the 2d MESFET allows direct illumination of the conductive channel from the top. The device demonstrates a broad photoresponse from at least 1.2 eV to 1.77 eV (0.7 μm to 1.06 μm) under top-illumination while under backside-illumination all light above 1.4 eV is absorbed by the semi-insulating GaAs substrate. Under top-illumination, the light is directly absorbed by the epitaxial GaAs, AlGaAs, and InGaAs layers, allowing for a broader photoresponse. Photogains as high as 2.4×10^7 were measured at 0.7 μm wavelength and 26 μW/cm² optical power intensity. A potentially exiting optoelectronic feature of this device is the ability to use the 2d MESFET as a high-gain, broad spectrum light detector with color discrimination capability due to the ability to tune the photoresponse of the device by varying the applied bias of the side gates. This feature is illustrated in Figure 5.

Digital Integrated Circuits

2d MESFET DCFL inverters have also been investigated. For inverters containing enhancement mode and depletion mode devices with threshold voltages of approximately 0.2 V and -0.1 V, respectively, voltage gains of 10 and noise margins near 0.25 V have been measured for supply voltages of 0.8 V to 1.0 V. Using AIM-Spice, a windows-based Spice routine with a customized 2d MESFET model, 11 stage ring oscillators were simulated from which power-delay products of less than 0.1 fJ were computed. This value represents an order of magnitude improvement compared to conventional technologies (see Figure 6). The transient simulations were based on the measured DC data plus an analytical capacitance-voltage model developed for the 2d MESFET.

Another exciting logic feature of the 2d MESFET is that the dual side-gates of the device may be biased independently in order to increase the functionality of 2d MESFET logic gates. Both NOR gate and NAND gate operation may be obtained with only two transistors by applying a constant reference voltage to one of the gates. This multi-functionality logic signifies a potentially major reduction in layout area, allowing for much more dense electronics. For example, AIM-Spice simulations suggest that D flip-flops may be implemented with only 18 2d MESFETs compared to 27 devices required using conventional GaAs MESFETs. In addition, lower power dissipation per gate signifies that thermal problems normally associated with dense circuitry may not be problematic for heterodimensional technology.

Other characterization studies of the 2d MESFET suggest that the device has a reduced temperature dependence compared to conventional GaAs MESFETs, indicating that 2d MESFET ICs will operate in a wider range of temperatures. Also, a study of the gate current suggests that the novel geometry of the 2d MESFET actually enhances the effective Schottky barrier height to the InGaAs quantum well layer, thereby reducing the gate leakage current normally associated with metal/InGaAs contacts. Thus, 2d MESFET ICs may realize the high speed material advantages of InGaAs but still maintain permissible levels of gate leakage. Finally, off-state breakdown, which is a major limiting factor in the voltage swing, output power, and reliability of both analog and digital circuits, has been measured to be on the order of 20 V for the 2d MESFET, demonstrating the robustness of the device.

Future Directions

Researchers at the University of Virginia, Rensselaer Polytechnic Institute, Hokkaido University, and Advanced Device Technologies continue to work on developing heterodimensional devices. The devices are interesting both from an experimental perspective, due to their distinctive characteristics including superior electron quantum confinement and high breakdown behavior, as well as from a commercial perspective, due to the enormous potential these devices hold for optoelectronic, microwave, and low power integrated circuit applications. In particular, since the epitaxial layers of the 2d MESFET are compatible with commercial HFET or PHEMT structures, it is possible to monolithically integrate 2d MESFETs and standard PHEMTs on the same wafer. The extension of heterodimensional transistor technology to other material heterostructures, such as InAlAs, SiGe, or GaN, is also possible. Alternatively, 2d MESFETs may be fabricated on bulk ion implanted n-GaAs. In this case a thin, shallow n-type implant is used as the conducting layer to form a quasi-two-dimensional electron gas layer. The use of ion implanted bulk material is appealing since it is compatible with commercial GaAs fabrication processes. Work on the 2d MESFET photodetector and multi-channel microwave 2d MESFET are both in their fledgling stages and present ample opportunities for device optimization. Fabrication of low power heterodimensional ICs is on-going; however, many fabrication issues related to lay-out and interconnections must be resolved before commercial 2d MESFET ICs may be produced. In short, much more work remains to be done for this emerging new technology, but the potential rewards are numerous and worthwhile.

Suggested reading

P.J. Koh, W.C.B. Peatman, and T.W. Crowe, "Millimeter Wave Tripler Evaluation of a Metal/2-DEG Schottky Diode Varactor," *IEEE Microwave and Guided Wave Letters*, vol. 5, pp. 73-75, 1995.

W. C. B. Peatman, M. Hurt, H. Park, T. Ytterdal, R. Tsai, and M. Shur, "Narrow Channel 2-D MESFET for Low Power Electronics," *IEEE Transactions on Electron Devices*, Vol. 42, No. 9, pp. 1569-1573, Sept. 1995.

H. Okada, T. Hashizume, and H. Hasegawa, "Transport Characterization of Schottky In-Plane Gate Al0.3Ga0.7As/GaAs Quantum Wire Transistors Realized by *In-Situ* Electrochemical Process," *Jpn. J. Appl. Phys.*, Vol. 34, Pt. 1, No. 12B, 1995.

R. Tsai, F. Schuermeyer, W. C. B. Peatman, and M. Shur, "The Optoelectronic Response of a Laterally Contacted 2-D MESFET," *IEEE Transactions on Electron Devices*, Vol. 43, No. 12, pp. 2300-2301, Dec. 1996.

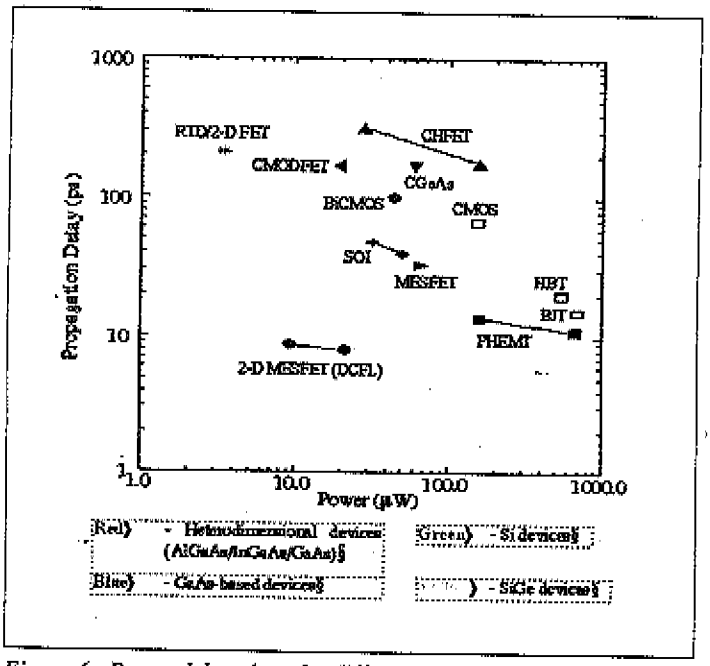

Figure 6. Power-delay chart for different technologies representative of the state-of-the-art. AIM-Spice simulations of the 2d MESFET predict an order of magnitude improvement in the power-delay product compared to conventional technologies.